hmp limited

PUMA 2/77F16006/A - 70/90/12

Issue 5.0 November 1999

Description

Available in PGA (PUMA 2) and Gullwing (PUMA77) footprints.

The PUMA **F16006 is a 16MBit FLASH module user configurable as 512K x 32, 1M x 16 or 2M x 8. The device is available with access times of 70, 90 and 120ns.

The device utilises, 5V only FLASH, to simplify circuit design. Sector size is 64K Byte with hardware protection available on any number of sectors.

The device features 10,000 Write erase cycle compatibility and 10 year data retention.

All options may be screened in accordance with MIL-STD-883.

Features

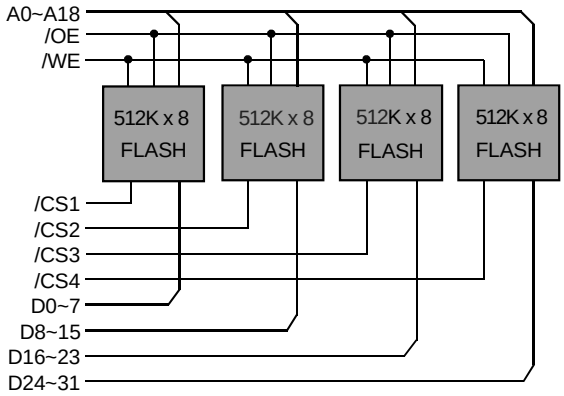
- 16 Megabit FLASH module.
- Fast Access Times of 70/90/120 ns.
- Output Configurable as 32 / 16 / 8 bit wide.
- Operating Power 880/456/242mW (Max).
  Low Power Standby 33mW (Max).
- Automatic Write/Erase by Embedded Algorithm - end of Write/Erase indicated by /DATA Polling and Toggle Bit.
- Flexible Sector Erase Architecture - 64K byte sector size, with hardware protection of any number of sectors.
- Erase/Write Cycle Endurance 100,000 (Min.) - E variant.
- 10 year Data Retention.
- May be screened in accordance with MIL-STD-883.

Package Details

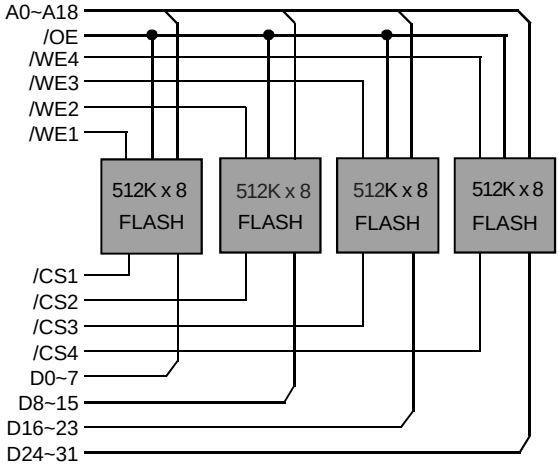
PUMA 2 -JEDEC 66 pin Ceramic PGA Package.
Max. Dimensions (mm) - 27.69 x 27.69 x 6.86
PUMA 77 -JEDEC 68 Leaded GullWing Package
Max. Dimensions (mm) - 25.15 x 25.15 x 5.44

Block Diagram

PUMA 77F16006



PUMA 2F16006, 77F16006A



Pin Definitions

See page 2.

Pin Functions

Description	Signal
Address Input	A0~A18
Data Input/Output	D0~D31
Chip Select	/CS1~4
Write Enable	/WE1~4
Output Enable	/OE
No Connect	NC
Power	V_{CC}
Ground	V_{SS}

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Pin Definitions

PUMA77F16006

Pin	Signal	Pin	Signal
1	V_{SS}	35	/OE
2	/CS3	36	/CS2
3	A5	37	A17
4	A4	38	NC
5	A3	39	NC
6	A2	40	NC
7	A1	41	A18
8	A0	42	V_{SS}
9	NC	43	NC
10	D0	44	D31
11	D1	45	D30
12	D2	46	D29
13	D3	47	D28
14	D4	48	D27
15	D5	49	D26
16	D6	50	D25
17	D7	51	D24
18	V_{SS}	52	V_{SS}
19	D8	53	D23
20	D9	54	D22
21	D10	55	D21
22	D11	56	D20
23	D12	57	D19
24	D13	58	D18
25	D14	59	D17
26	D15	60	D16
27	V_{CC}	61	V_{CC}
28	A11	62	A10
29	A12	63	A9
30	A13	64	A8
31	A14	65	A7
32	A15	66	A6
33	A16	67	/WE
34	/CS1	68	/CS4

PUMA2F16006

Pin	Signal	Pin	Signal
1	D8	34	D24
2	D9	35	D25
3	D10	36	D26
4	A14	37	A7
5	A16	38	A12
6	A11	39	A18
7	A0	40	A13
8	NC	41	A8
9	D0	42	D16
10	D1	43	D17
11	D2	44	D18
12	/WE2	45	V_{CC}
13	/CS2	46	/CS4
14	V_{SS}	47	/WE4
15	D11	48	D27
16	A10	49	A4
17	A9	50	A5
18	A15	51	A6
19	V_{CC}	52	/WE3
20	/CS1	53	/CS3
21	NC	54	V_{SS}
22	D3	55	D19
23	D15	56	D31
24	D14	57	D30
25	D13	58	D29
26	D12	59	D28
27	/OE	60	A1
28	A17	61	A2
29	/WE1	62	A3
30	D7	63	D23
31	D6	64	D22
32	D5	65	D21
33	D4	66	D20

PUMA77F16006A

Pin	Signal	Pin	Signal
1	V_{SS}	35	/OE
2	/CS3	36	/CS2
3	A5	37	A17
4	A4	38	/WE2
5	A3	39	/WE3
6	A2	40	/WE4
7	A1	41	A18
8	A0	42	V_{SS}
9	NC	43	NC
10	D0	44	D31
11	D1	45	D30
12	D2	46	D29
13	D3	47	D28
14	D4	48	D27
15	D5	49	D26
16	D6	50	D25
17	D7	51	D24
18	V_{SS}	52	V_{SS}
19	D8	53	D23
20	D9	54	D22
21	D10	55	D21
22	D11	56	D20
23	D12	57	D19
24	D13	58	D18
25	D14	59	D17
26	D15	60	D16
27	V_{CC}	61	V_{CC}
28	A11	62	A10
29	A12	63	A9
30	A13	64	A8
31	A14	65	A7
32	A15	66	A6
33	A16	67	/WE1
34	/CS1	68	/CS4

Absolute Maximum Ratings(1)

Parameter	Symbol	Min	Typ	Max	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.6	-	+6.0	V
Supply Voltage(2)		-0.6	-	+6.0	V
Voltage on A9 relative to V_{SS}(3)	V_{A9}	-0.6	-	+13.5	V
Storage Temperature	T_{STG}	-65	-	+150	^{O}C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied.

(2) Minimum DC voltage on any input or I/O pin is -0.5V. Maximum DC voltage on output and I/O pins is V_{CC}+0.5V During transitions voltage may overshoot by ±2V for up to 20ns

(3) Minimum DC input voltage on A9 is -0.5V during voltage transitions, A9 may overshoot V_{SS} to -2V for periods of up to 20ns, maximum DC input voltage in A9 is 13.5V which may overshoot to 14.0V for periods up to 20ns

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit	
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	
Input High Voltage		V_{IH}	2.0	-	V_{CC}+0.5	V	
Input Low Voltage		V_{IL}	-0.5	-	0.8	V	
Operating Temperature	(Commercial)	T_A	0	-	70	^{O}C	
	(Industrial)	T_{AI}	-40	-	85	^{O}C	(I Suffix)
	(Military)	T_{AM}	-55	-	125	^{O}C	(M\MB Suffix)

DC Electrical Characteristics

(V_{CC}=5V±10%, T_A=-55^{O}C to 125^{O}C)

Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current Address, /OE		I_{LI1}	V_{CC}=V_{CC}max, V_{IN}=0V or V_{CC}	-	-	±10	µA
A9 Input Leakage Current		I_{LI2}	V_{CC}=V_{CC}max, A9=12.5V	-	-	400	µA
Output Leakage Current		I_{LO}	V_{CC}=V_{CC}max, V_{OUT}=0V or V_{CC}	-	-	±10	µA
V_{CC} Operating Current	32 Bit	I_{CCO32}	/CS(1)=V_{IL},/OE=V_{IH},I_{OUT}=0mA, f=6MHz	-	-	160	mA
	16 Bit	I_{CCO16}	As Above	-	-	83	mA
	8 Bit	I_{CCO8}	As Above	-	-	44	mA
V_{CC} Program Erase Current	32 Bit	I_{CCP32}	Programming In Progress	-	-	240	mA
	16 Bit	I_{CCP16}	As Above	-	-	123	mA
	8 Bit	I_{CCP8}	As Above	-	-	64	mA
Standby Supply Current		I_{SB1}	V_{CC}=V_{CC}max,/CS=V_{IH}(1) /OE=V_{IH}	-	-	6	mA
Autoselect/Sector Protect Voltage		V_{ID}	V_{CC}=5.0V	11.5	-	12.5	V
Output Voltage Low		V_{OL}	I_{OL}=12mA, V_{CC} = V_{CC} Min	-	-	0.45	V
Output Voltage High		V_{OH1}	I_{OH}=-2.5mA, V_{CC} = V_{CC} Min	2.4	-	-	V
Low V_{CC} Lock-Out Voltage		V_{LKO}		3.2	-	4.2	V

Notes (1) /CS1~4 inputs operate simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

Capacitance

(V_{CC} = 5.0V, T_A = 25^{O}C, F=1MHz.)

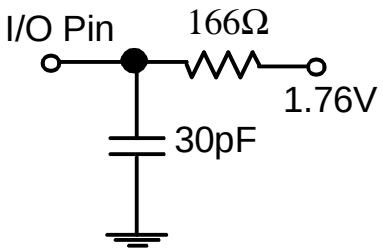
Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Input Capacitance	(Address, /OE,)	C_{IN1}	V_{IN}=0V	-	-	30	pF
	Other Pins	C_{IN2}	V_{IN}=0V	-	-	12	pF
Output Capacitance	32 bit mode	C_{OUT32}	V_{OUT}=0V	-	-	56	pF

Note : These Parameters are calculated not measured.

Test Conditions

- Input pulse levels : 0V to 3.0V
- Input rise and fall times : 5ns
- Input and Output timing reference levels : 1.5V
- Output Load : See Load Diagram.
- Module tested in 32 bit mode.
- V_{CC} = 5V±10%

Output Load



Read Cycle

		70		90		120		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Address Valid to Next Address Valid.	t_{RC}	70	-	90	-	120	-	ns
Address Valid to Output Valid	t_{ACC}	70	-	90	-	120	-	ns
Chip Select Low to Output Transition	t_{LZ}	0	-	0	-	0	-	ns
Chip Select Low to Output Valid	t_{CS}	-	70	-	90	-	120	ns
Output Enable Low to Output Transition	t_{OLZ}	0	-	0	-	0	-	ns
Output Enable Low to Output Valid	t_{OE}	-	35	-	45	-	50	ns
Chip Enable High to Output High-Z	t_{HZ}	-	20	-	25	-	30	ns
Output Enable High to Output High Z	t_{DF}	-	20	-	25	-	30	ns
Chip Select, Output Enable or Address Transition to Output Transition	t_{OH}	0	-	0	-	0	-	ns

Write/Erase/Program

		70		90		120		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Address Valid to Next Address Valid	t_{WC}	70	-	90	-	120	-	ns
Chip Select Low to Write Enable Low	t_{CS}	0	-	0	-	0	-	ns
Write Enable Low to Write Enable High	t_{WP}	45	-	50	-	55	-	ns
Input Valid to Write Enable High	t_{DS}	30	-	35	-	40	-	ns
Write Enable High to Input Transition	t_{DH}	0	-	0	-	0	-	ns
Write Enable High to Chip Select High	t_{CH}	0	-	0	-	0	-	ns
Write Enable High to Chip Select Low	t_{WPH}	20	-	20	-	20	-	ns
Address Valid to Write Enable Low	t_{AS}	0	-	0	-	0	-	ns
Write Enable Low to Address Transition	t_{AH}	45	-	50	-	55	-	ns
Output Enable High to Write Enable Low	t_{GHWL}	0	-	0	-	0	-	ns
Write Enable High to Output Enable Low	t_{OEH}	0	-	0	-	0	-	ns
VCC High to Chip Enable Low	t_{VCS}	50	-	50	–	50	–	µs

Notes :See Overleaf.

Erase/Program Alternate /CS controlled Writes

		70		90		120		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Address Valid to Next Address Valid	t_{WC}	70	-	90	-	120	-	ns
Write Enable Low to Chip Select Low	t_{WS}	0	-	0	-	0	-	ns
Chip Select Low to Chip Select High	t_{CP}	45	-	50	-	55	-	ns
Input Valid to Chip Select High	t_{DS}	30	-	35	-	40	-	ns
Chip Select High to Input Transition	t_{DH}	0	-	0	-	0	-	ns
Chip Select High to Write Enable High	t_{WH}	0	-	0	-	0	-	ns
Chip Select High to Chip Select Low	t_{CPH}	20	-	20	-	20	-	ns
Address Valid Chip Select Low	t_{AS}	0	-	0	-	0	-	ns
Chip Select Low to Address Transition	t_{AH}	45	-	50	-	55	-	ns
Output Enable High Chip Select Low	t_{GHEL}	0	-	0	-	0	-	ns
Chip Enable High to Output Enable Low	t_{OEH}	0	-	0	-	0	-	ns
V_{CC} High to Write Eanble Low	t_{VCS}	50	-	50	-	50	-	µs

Notes : (1) This does not include the preprogramming time.
(2) These timings are for Sector Protect and Unprotect operations.
(3) This timing is for Sector Unprotect only.
(4) Not 100% tested.

Figure 1 - Read Mode

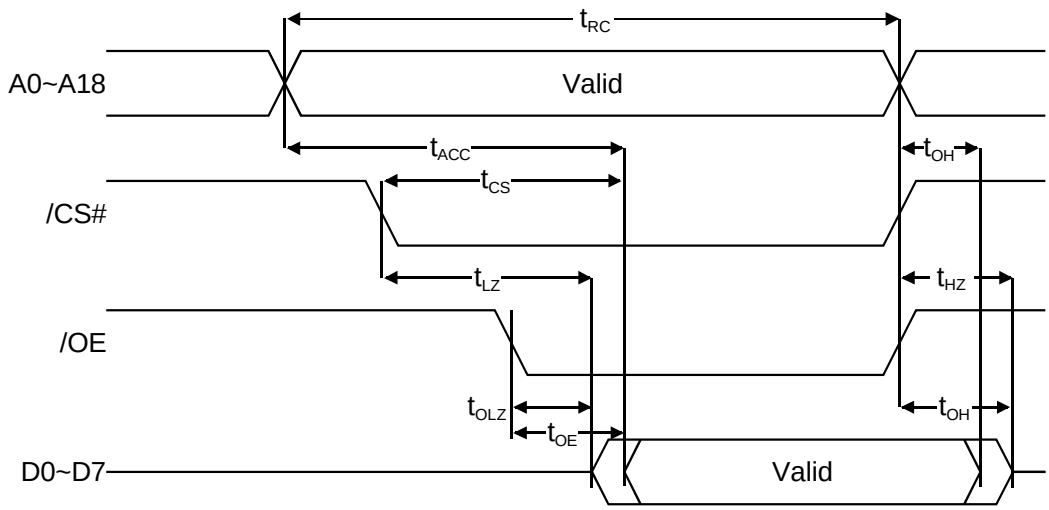


Figure 2 - Write AC Waveform

/WE Controlled

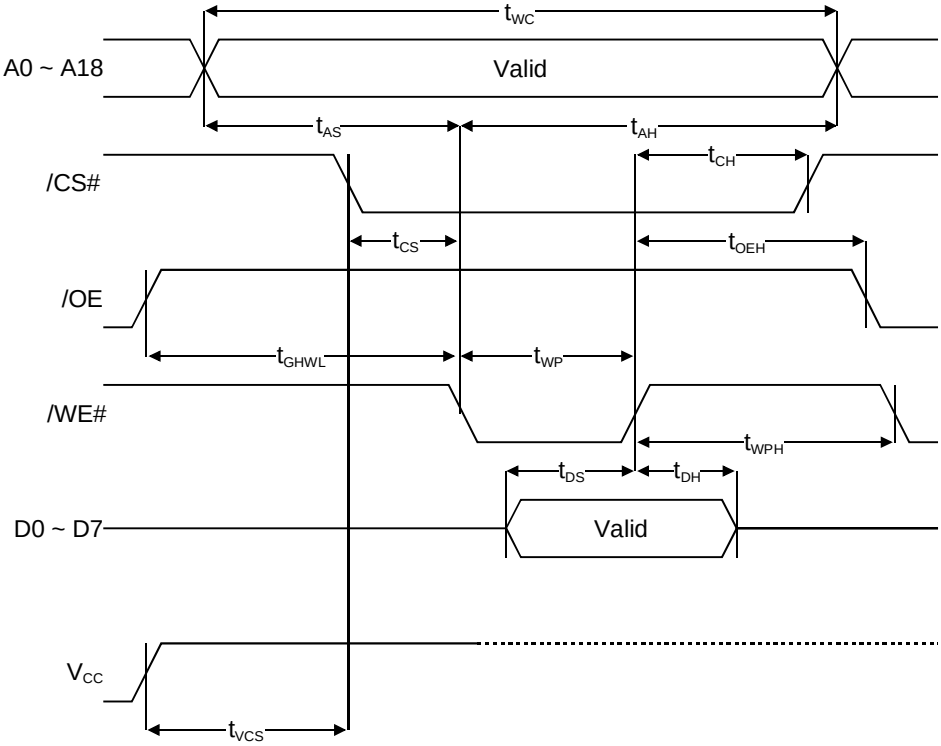


Figure 3 - Write AC Waveforms

/CS Controlled

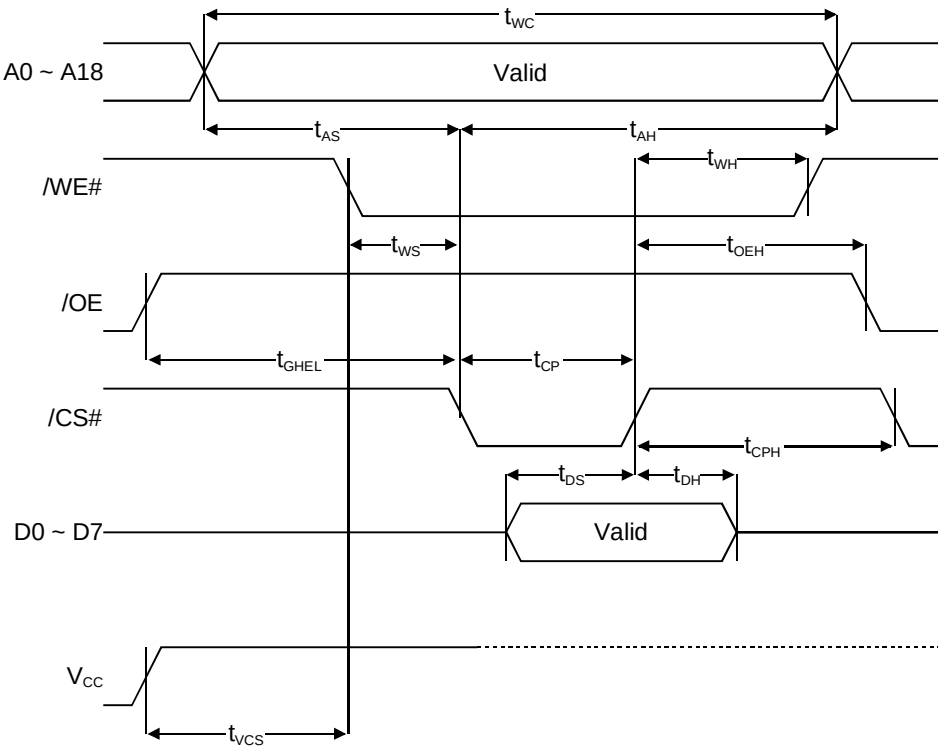


Figure 4 - Data Polling

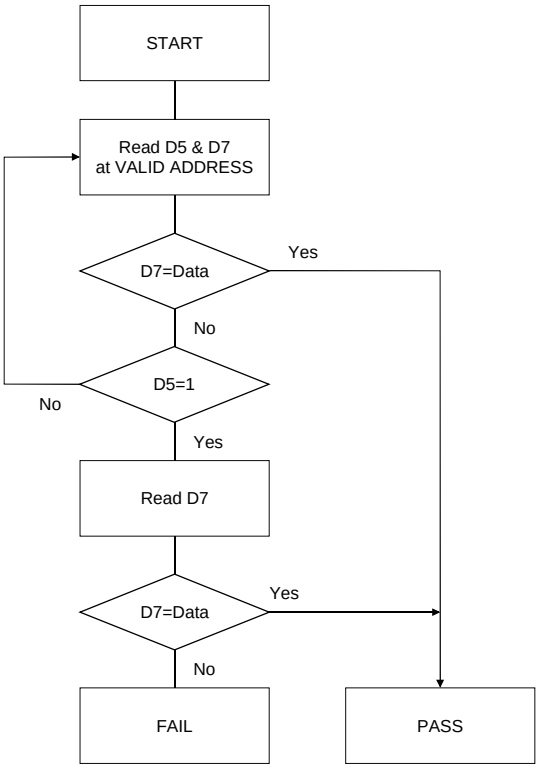
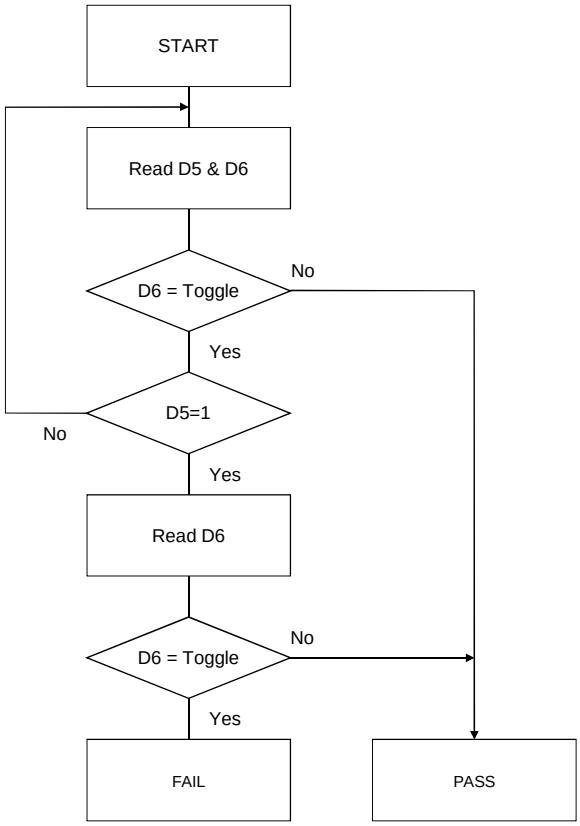


Figure 5 - Data Toggle



There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby. See Table 2, Bus Operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Bus Read

Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 1, Read Mode AC Waveforms, and Read AC Characteristics, for details of when the output becomes valid.

Bus Write

Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figures 2 and 3, Write AC Waveforms, and Write AC Characteristics, for details of the timing requirements.

Output Disable

The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

Standby

When Chip Enable is High, V_{IH}, the Data Inputs/Outputs pins are placed in the high impedance state and the Supply Current is reduced to the Standby level. When Chip Enable is at V_{IH} the Supply Current is reduced to the TTL Standby Supply Current, I_{SB1}. For Standby current levels see DC Characteristics. During program or erase operations the memory will continue to use the Program/Erase Supply Current, I_{CCP}, for Program or Erase operations until the operation completes.

Special Bus Operations

Additional bus operations can be performed to read the Electronic Signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

Electronic Signature

The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Table 2, Bus Operations.

Block Protection and Blocks Unprotection

Each block can be separately protected against accidental Program or Erase. Protected blocks can be unprotected to allow data to be changed. Block Protection and Blocks Unprotection operations must only be performed on programming equipment.

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security. The commands are summarized in Table 4, Commands. Refer to Table 4 in conjunction with the text descriptions below.

Read/Reset Command

The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

If the Read/Reset command is issued during a Block Erase operation or following a Programming or Erase error then the memory will take up to 10µs to abort. During the abort period no valid data can be read from the memory. Issuing a Read/Reset command during a Block Erase operation will leave invalid data in the memory.

Auto Select Command

The Auto Select command is used to read the Block Protection Status. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until another command is issued. The Block Protection Status of each block can be read using a Bus Read operation with A0 = V_{IL}, A1 = V_{IH}, and A16, A17 and A18 specifying the address of the block. The other address bits may be set to either V_{IL} or V_{IH}. If the addressed block is protected then 01h is output on the Data Inputs / Outputs, otherwise 00h is output.

Program Command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 5. Bus Read operations during the program operation will output the Status Register on the Data Inputs/ Outputs. See the section on the Status Register for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1' and attempting to do so will cause an error. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Unlock Bypass Command

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory. When the access time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock By-pass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

Unlock Bypass Program Command

The Unlock Bypass Program command can be used to program one address in memory at a time. The command requires two Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller. The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. A protected block cannot be programmed; the operation cannot be aborted and the Status Register is read. Errors must be reset using the Read/Reset command, which leaves the device in Unlock By-pass Mode. See the Program command for details on the behavior.

Unlock Bypass Reset Command

The Unlock Bypass Reset command can be used to return to Read/ Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command.

Chip Erase Command

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored. During the erase operation the memory will ignore all commands. It is not possible to issue any command to abort the operation. Typical chip erase times are given in Table 5. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase Command sets all of the bits in unprotected blocks of the memory to '1'. All previous data is lost.

Block Erase Command

The Block Erase command can be used to erase a list of one or more blocks. Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. The Block Erase operation starts the Program/Erase Controller about 50µs after the last Bus Write operation. Once the Program/Erase Controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. The Status Register can be read after the sixth Bus Write operation. See the Status Register for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend and Read/Reset commands. Typical block erase times are given in Table 5. All Bus Read operations during the Block Erase operation will output the Status Register on the Data Inputs/ Outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to re-set the error condition and return to Read mode.

The Block Erase Command sets all of the bits in the unprotected selected blocks to '1'. All previous data in the selected blocks is lost.

Erase Suspend Command

The Erase Suspend Command may be used to temporarily suspend a Block Erase operation and return the memory to Read mode. The The Program/Erase Controller will suspend within 15µs of the Erase Suspend Command being issued. Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/ Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume Command is issued. It will not be possible to select any further blocks for erasure after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program operations behave as normal on these blocks. Reading from blocks that are being erased will output the Status Register. It is also possible to enter the Auto Select mode: the memory will behave as in the Auto Select mode on all blocks until a Read/Reset command returns the memory to Erase Suspend mode.command requires one Bus Write operation.

Erase Resume Command

The Erase Resume command must be used to restart the Program/ Erase Controller from Erase Suspend. An erase can be suspended and resumed more than once.

Bus Read operations from any address always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed. The bits in the Status Register are summarized in Table 3, Status Register Bits.

Data Polling Bit (D7)

The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling Bit is output on D7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to D7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output D7, not its complement.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of D7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling Bit will output a '1' during a Bus Read operation within a block being erased. The Data Polling Bit will change from a '0' to a '1' when the Program/Erase Controller has suspended the Erase operation.

Figure 4, Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.

Toggle Bit (D6)

The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle Bit is output on D6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle Bit will output when addressing a cell within a block being erased. The Toggle Bit will stop toggling when the Program/Erase Controller has suspended the Erase operation.

Figure 5, Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.

Error Bit (D5)

The Error Bit can be used to identify errors detected by the Program/ Erase Controller. The Error Bit is set to '1' when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on D5 when the Status Register is read.

Note that the Program command cannot change a bit set at ’0’ back to ’1’ and attempting to do so willcause an error. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

Erase Timer Bit (D3)

The Erase Timer Bit can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/ Erase Controller starts erasing the Erase Timer Bit is set to ’1’. Before the Program/Erase Controller starts the Erase Timer Bit is set to ’0’ and additional blocks to be erased may be written to the Command Interface. The Erase Timer Bit is output on D3 when the Status Register is read.

Alternative Toggle Bit (D2)

The Alternative Toggle Bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle Bit is output on D2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle Bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations from addresses within the blocks being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle Bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode. After an Erase operation that causes the Error Bit to be set the Alternative Toggle Bit can be used to identify which block or blocks have caused the error. The Alternative Toggle Bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle Bit does not change if the addressed block has erased correctly.

Table 1 : Block Addresses

Size (Kbytes)	Address Range
64	70000h ~ 7FFFFh
64	60000h ~ 6FFFFh
64	50000h ~ 5FFFFh
64	40000h ~ 4FFFFh
64	30000h ~ 3FFFFh
64	20000h ~ 2FFFFh
64	10000h ~ 1FFFFh
64	00000h ~ 0FFFFh

Table 2 : Bus Operations

Operation	/CS	/OE	/WE	Address Inputs	Data I/O
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	High Z
Standby	V_{IH}	X	X	X	High Z

Note : X=V_{IL} or V_{IH}

Table 3 : Status Register Bits

Operation	Address	D7	D6	D5	D3	D2
Program	Any Address	/D7	Toggle	0	-	-
Program During Erase Suspend	Any Address	/D7	Toggle	0	-	-
Program Error	Any Address	D7	Toggle	1	-	-
Chip Erase	Any Address	0	Toggle	0	1	Toggle
Block Erase before timeout	Erasing Block	0	Toggle	0	0	Toggle
	Non Erasing Block	0	Toggle	0	0	No Toggle
Block Erase	Erasing Block	0	Toggle	0	1	Toggle
	Non Erasing Block	0	Toggle	0	1	No Toggle
Erase Suspend	Erasing Block	1	No Toggle	0	1	Toggle
	Non Erasing Block	Data read as normal				
Erase Error	Good Block Address	0	Toggle	1	1	No Toggle
	Faulty Block Address	0	Toggle	1	1	Toggle

Note : Unspecified Bits should be ignored

Table 4 : Commands

Command	Length	Bus Write Operations											
		First		Second		Third		Fourth		Fifth		Sixth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read / Reset	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Autoselect	3	555	AA	2AA	55	555	90						
Program	4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass	3	555	AA	2AA	55	555	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase	6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Erase Suspend	1	X	B0										
Erase Resume	1	X	30										

Note : *X : Don't Care, PA : Program Address, PD : Program Data, BA : Any address in the Block. All values in the table are in hexadecimal.*
The Command Interface only uses address bits A0-A10 to verify the commands, the upper address bits are Don't Care.

Read/Reset.
After a Read/Reset command, read the memory as normal until another command is issued.

Auto Select.
After an Auto Select command, read Manufacturer ID, Device ID or Block Protection Status.

Program, Unlock Bypass Program, Chip Erase, Block Erase.
After these commands read the Status Register until the Program/Erase Controller completes and the memory returns to Read Mode. Add additional Blocks during Block Erase Command with additional Bus Write Operations until the Timeout Bit is set.

Unlock Bypass.
After the Unlock Bypass command issue Unlock Bypass Program or Unlock Bypass Reset commands.

Unlock Bypass Reset.
After the Unlock Bypass Reset command read the memory as normal until another command is issued.

Erase Suspend.
After the Erase Suspend command read non-erasing memory blocks as normal, issue Auto Select and Program commands on non-erasing blocks as normal.

Erase Resume.
After the Erase Resume command the suspended Erase operation resumes, read the Status Register until the Program/Erase Controller completes and the memory returns to Read Mode.

Table 5 - Program, Erase Times and Program, Erase Endurance Cycles

(T_A= 0 to 70^{O}C, -40 to 85^{O}C or -40 to 125^{O}C)

Parameter	Min	Typ(1)	Typical after 100K W/E Cycles(1)	Max	Unit
Chip Erase (All bits in memory set to '0')		1.5	1.5		sec
Chip Erase		5	5	20	sec
Block Erase (64 Kbytes)		0.6	0.6	4	sec
Program		8	8	150	µs
Chip Program		4.5	4.5	18	sec
Program/Erase Cycles (per Block)	10,000				Cycles

Note : T_A=25^{O}C, V_{CC}=5V.

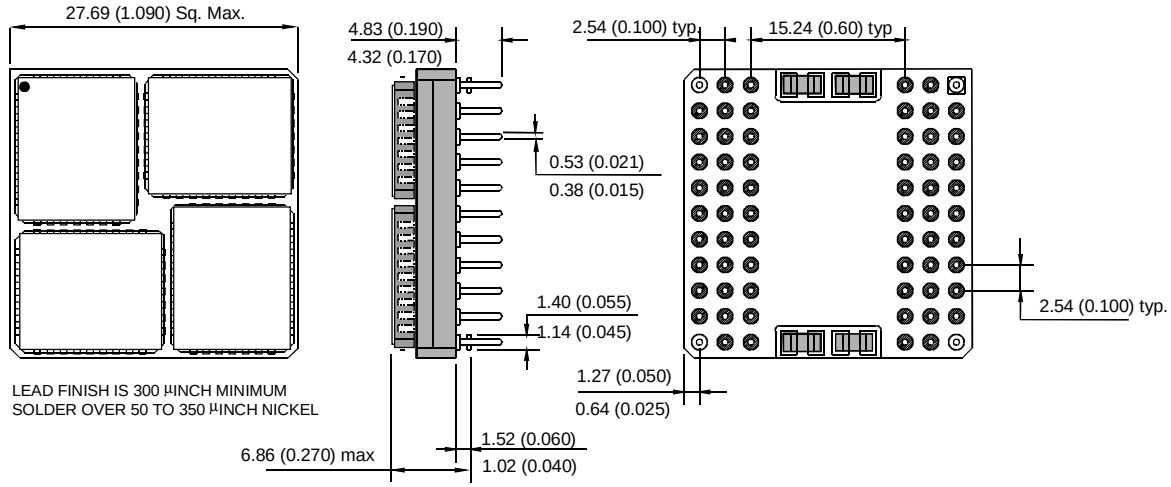
Military Screening Procedure

For High Reliability product in accordance with Mil-883 Method 5004 Shown Below

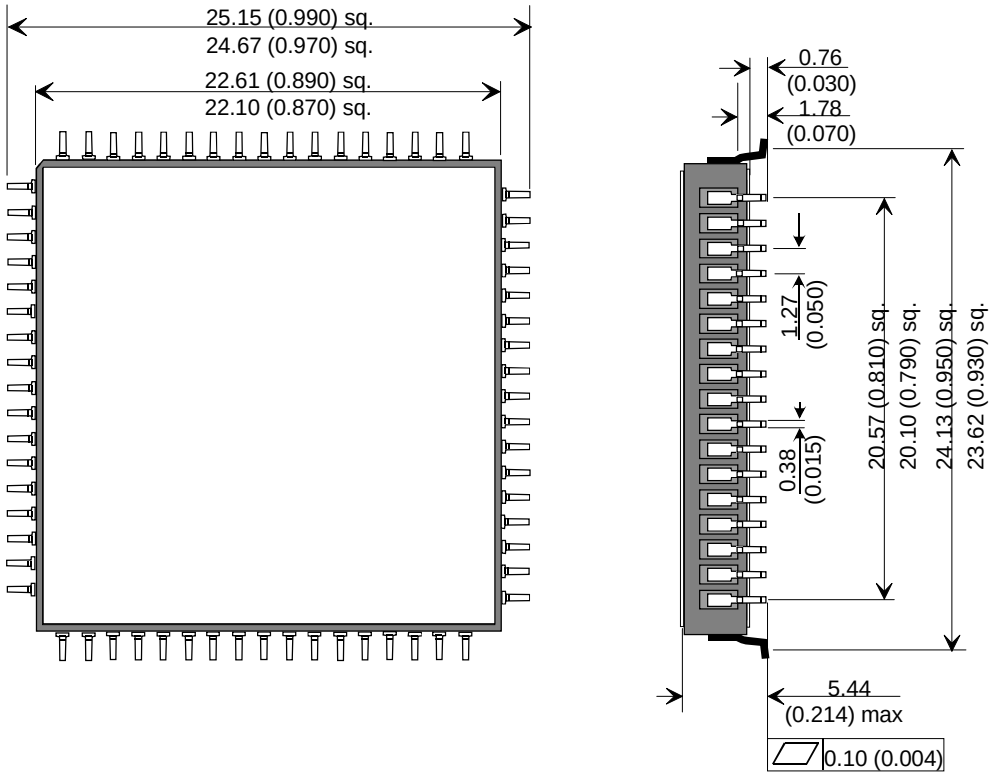
PUMA 77 MB Grade Multi Chip Module Screening Flow		
Screen	Test Method	Level
Visual Mechanical		
Internal Visual	2017 Codition B or manufacturers equivalent	100%
Temperature Cycle	1010 Condition B (10 cycles, -65^{O}C to +150^{O}C)	100%
Constant Acceleration	2001 Condition E (Y, only) (10,000g)	100%
Burn In		
Pre-Burn-In electrical	Per applicable device specifications at T_A=+25^{O}C	100%
Burn-In	Method 1015,Condition D,T_A=+125^{O}C,160hrs min	100%
Final Electrical Tests	Per Applicable Device Specification	
Static (dc)	a) @T_A=+25^{O}C and power supply extremes	100%
	b) @temperature and power supply extremes	100%
Functional	a) @T_A=+25^{O}C and power supply extremes	100%
	b) @temperature and power supply extremes	100%
Switching (ac)	a) @T_A=+25^{O}C and power supply extremes	100%
	b) @temperature and power supply extremes.	100%
Percent Defective Allowable (PDA)	Calculated at post-burn-in at T_A=+25^{O}C	10%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
Quality Conformance	Per applicable device specifications	Sample
External Visual	2009 Per Vendor or Customer Specification	100%

PUMA 2 MB Component Screening Flow		
Screen	Test Method	Level
Visual Mechanical		
External Visual	17 Condition B or manufacturers equivalent	100%
Temperature Cycle	1010 Condition C (10 cycles, -65^{O}C to +150^{O}C)	100%
Burn In		
Pre-Burn-In electrical	Per applicable device specifications at T_A=+25^{O}C	100%
Burn-In	Method 1015,Condition D,T_A=+125^{O}C,160hrs min	100%
Final Electrical Tests	Per Applicable Device Specification	
Static (dc)	a) @T_A=+25^{O}C and power supply extremes	100%
	b) @temperature and power supply extremes	100%
Functional	a) @T_A=+25^{O}C and power supply extremes	100%
	b) @temperature and power supply extremes	100%
Switching (ac)	a) @T_A=+25^{O}C and power supply extremes	100%
	b) @temperature and power supply extremes.	100 %
Percent Defective Allowable (PDA)	Calculated at post-burn-in at T_A=+25^{O}C	5%
Quality Conformance	Per Applicable Device Specification	Sample
External Visual	2009 Per Vendor or Customer Specification	100%

PUMA 2 - JEDEC 66 pin Ceramic PGA.



PUMA 77 - JEDEC 68 Leaded Ceramic Gullwing Package.



Ordering Information

PUMA 2F16006AMB - 70E

Speed	70	=	70ns
	90	=	90ns
	120	=	120ns
Temp. Range/Screening	Blank	=	Commercial
	I	=	Industrial
	M	=	Military
	MB	=	Processed in accordance with MIL-STD-883
/WE Option	Blank	=	Single /WE (PUMA 77only) /WE1~4 (PUMA 2 only)
	A	=	/WE1~4 (PUMA77 only)
Memory Organisation	16006	=	512K x 32 configurable as 1M x 16, and 2M x 8
Technology	F	=	FLASH
Package	PUMA 2	=	JEDEC 66 Pin Ceramic PGA Package
	PUMA77	=	JEDEC 68 Leaded Gull Wing Surface Mount Ceramic Package

Note : E is designated to parts with extended Erase/Write Cycle Endurance (100,000 Min.)
If not specified when ordered only a Erase/Write Cycle Endurance of 10,000 can be guaranteed